IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Appellant:			
Paul Rudolf			
Filed:	August 26, 2003	Art Unit:	2129
Serial No.:	10/648,855	Examiner:	Hirl, Joseph P.
		Docket No.:	121306.00002 (128988.00002)
For:	ASSOCIATIVE MEMORY DEVICE AND METHOD BASED ON WAVE PROPAGATION		

APPEAL BRIEF

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APPELLANT'S BRIEF (37 C.F.R. 4 1.37)

This brief is in furtherance of the Notice of Appeal, filed in this case on March 6, 2007 and received by the U.S. Patent and Trademark Office on March 9, 2007.

The fees required under §1.17(c), and any required petition for extension of time for filing this brief and related fees are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

The final page of this brief bears the practitioner's signature.

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I. REAL PARTY OF INTEREST (37 C.F.R. § 41.37(c)(1))

The real party in interest in this appeal is Paul Rudolf, the inventor of the patent application.

II. RELATED APPEALS AND INTERFERENCES (37 C.F.R. § 41.37(c)(2))

There are no such appeals or interferences.

III. STATUS OF CLAIMS (37 C.F.R. § 41.37(c)(3))

The status of the claims in this application are:

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are: 78 claims. (Claims 1-78)

Claims currently pending in the application: 78 pending claims

B. STATUS OF ALL THE CLAIMS

1. Claims cancelled: None

2. Claims withdrawn from consideration but not cancelled: None

3. Claims pending: 1-78

4. Claims allowed: NONE.

5. Claims rejected: 1-78

C. CLAIMS ON APPEAL

The claims on appeal are: 1-78.

IV. STATUS OF AMENDMENTS (37 C.F.R. § 41.37(c)(4))

The claims presently pending are those submitted September 26, 2006, in response to the non-final Office Action mailed May 26, 2006.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER (37 C.F.R. § 41.37(c)(5))

The following summary is provided without any intention to limit the scope of the claims. The subject matter of claims 1-78 is summarized below.

Claim 1 includes an associative memory device, comprising: an input device for accepting a set or a plurality of sets of input information; one or a plurality of input buffers; the input device being coupled to, or integrated into, the input buffer; a means for transporting the input information to the input buffer; the input buffer being adapted to transform the input information into corresponding sets of complex-valued wave fields as wave-modeled input data; one or a plurality of recording structures, referred to as a cortex; the input buffer being further adapted to propagate the wave-modeled input data to the cortex; the cortex being adapted to associate the desired sets of wave-modeled input data through an invertible mathematical function or operation, thus creating one or a plurality of associations within the cortex; the cortex being further adapted to store the associations in a distributed manner across a cortex surface with other previously stored associations; the cortex being further adapted to form and store linear combinations of associations; an input device being operable to accept one or a plurality of retrieval prompts, referred to as a prompt; the input buffer being operable to transform the prompt into a corresponding set of complex-valued wave fields, as a wave-modeled prompt; the input buffer being operable to propagate the wave-modeled prompt to the cortex; the cortex being operable to cause the wave-modeled prompt to mathematically operate upon the previously stored associations using a de-association operation that is the inverse of that originally used to form the associations; the cortex being adapted to store the wave-modeled prompt with other previously stored associations and wave modeled prompts; a means for the result of the mathematical de-association operation, representing a wave-modeled retrieval, to propagate from the cortex to one or a plurality of output buffers, said output buffer being referred to with the input buffer as the buffers; the output buffer being operable to transform the wave-modeled retrieval into output data; and a means for using control data to provide overall control of the associative memory device. By way of example and not by limitation, see, e.g., Fig. 27 and the description of the components and functions of the components shown in Fig. 27 from page 82, line 12 to page 95, line 6 of the specification.

Claims 2 through 78 contain related limitations that are also shown by way of example

and not by limitation in Fig. 27 from page 82, line 12 to page 95, line 6 of the specification. The Applicant reserves the right to further address these claims in response to the Examiner's answer to the arguments presented herein.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL ((37 C.F.R. § 41.37(c)(6))

1. Whether the Examiner has made a proper objection to the Inventor.

2. Whether the Examiner has made a proper objection to the Specification.

3. Whether the Examiner has properly rejected the claims under 35 U.S.C. 101 for nonstatutory subject matter.

4. Whether the Examiner has properly rejected the claims under 35 U.S.C. 101 for lacking utility.

VII. ARGUMENTS ((37 C.F.R. § 41.37 (c)(7))

1. The Examiner has failed to make a proper objection to the Inventor.

The Examiner improperly asserts that a statement in a prior art reference requires correction of inventorship. As noted by the Federal Circuit, "a long line of decisions in this court holds that a person is a joint inventor only if he contributes to the **conception** of the claimed invention." *Eli Lilly and Co. v. Aradigm Corp.*, 376 F.3d 1352, 1359 (Fed. Cir. 2004) (emphasis added). The statement relied on by the Examiner at best suggests that others may have employed a variation of the Helmholtz-Kirchhoff equation to computer model a wide range of diffracting systems, but do not even establish that employing a variation of the Helmholtz-Kirchhoff equation to computer model a wide range of diffracting systems is any way related to the claimed invention, which is drawn to associative memory devices and a method of autonomous pattern recognition. As such, nothing in the cited passage evidences that the named persons contributed to the **conception** of the claimed invention. In response, the Examiner states that a cited passage from the specification "forms the conceptual basis for the embodiment utilizing software emulation of wave propagation." The Examiner is simply not able to state, relying only on the specification and publications, which person may have conceived the claimed invention – to do so would require the ability to read the minds of the persons involved with the conception and reduction to practice of the claimed invention. The alleged inventors are simply not inventors – the Applicant is aware of no facts that would mandate that any additional inventors be named, nor of any claim by such persons to be inventors of the pending claimed inventions. It would simply be improper to name persons as inventors who did not conceive of the claimed invention. Accordingly, this objected must be **REVERSED**.

2. The Examiner has made an improper objection to the Specification.

The Examiner improperly rejects the claims under the guise of an objection to the Specification. M.P.E.P. 2107.02 states that the "**claimed invention** is the focus of the assessment of whether an applicant has satisfied the utility requirement. **Each claim** (i.e. each "invention"), therefore, **must be evaluated on its own merits** for compliance with all statutory requirements." (Emphasis added). While the Examiner cites to selected excerpts from the

specification and states in conclusory fashion that the "specification [has] no utility" and that "the invention does not work and has no utility," it is the utility of the claims and not the specification that must be determined. The objection to the Specification on the basis that "the invention does not work and has no utility" is legal error, because the Examiner is not even considering the claims, each of which must be reviewed on its own merits. As no nexus has been shown between the alleged defects in the specification and the claimed inventions, the objection is improper and must be **REVERSED**.

3. The Examiner has improperly rejected the claims under 35 U.S.C. 101 for nonstatutory subject matter.

The Examiner's rejection of the claims under 35 U.S.C. 101 is legally deficient, and the Examiner does not even make a cursory attempt to address each claim to determine whether any of the claims are drawn to statutory subject matter. Instead, the Examiner relies on various phrases from selected (and unidentified) claims, as well as the ***Title of the Invention***! Such a cursory, conclusory and legally improper analysis merely confirms that the Examiner has failed to properly consider whether each claim is drawn to statutory subject matter.

In order to provide a valid legal basis for rejecting each claim under 35 U.S.C. 101, the claimed invention as a whole for each and every claim must be considered. Consider *AT&T Corp. v. Excel Communications, Inc.*, 172 F.3d 1352, 1357 (Fed. Cir. 1999), where the Federal Circuit explained that:

> The *State Street* formulation, that a mathematical algorithm may be an integral part of patentable subject matter such as a machine or process if **the claimed invention as a whole** is applied in a "useful" manner, follows the approach taken by this court en banc in *In re Alappat*, 33 F.3d 1526, 31 USPQ2d 1545 (Fed. Cir. 1994). In *Alappat*, we set out our understanding of the Supreme Court's limitations on the patentability of mathematical subject matter and concluded that: **[The Court] never intended to create an overly broad, fourth category of [mathematical] subject matter excluded from § 101**. Rather, at the core of the Court's analysis . . . lies an attempt by the Court to explain a rather straightforward concept, namely, that certain types of mathematical subject matter, ***standing alone***, represent nothing more than *abstract ideas until reduced to some type of practical application*, and thus that subject matter is not, in and of itself, entitled to patent protection. *Id.* at 1543, 31 USPQ2d at 1556-57 (emphasis added). Thus, **the *Alappat* inquiry simply requires an examination of the contested claims to see if the claimed subject matter as a whole is a disembodied mathematical concept representing nothing more than a "law**

> **of nature" or an "abstract idea," or if the mathematical concept has been reduced to some practical application rendering it "useful."** *Id.* at 1544, 31 USPQ2d at 1557. In *Alappat*, we held that more than an abstract idea was claimed because **the claimed invention as a whole** was directed toward forming a specific machine that produced the useful, concrete, and tangible result of a smooth waveform display. *See id.* at 1544, 31 USPQ2d at 1557.

(Emphasis added). As such, it is apparent that the utility of the claimed invention as a whole must be the subject of the enquiry into the patentability of the claimed inventions under 35 U.S.C. 101. Ignoring those parts of the claim that are drawn to a practical application and only focusing on claim elements that, if they were claimed alone, *might* be properly rejected under 35 U.S.C. 101, is simply improper.

Consider claim 1, which is drawn to an associative memory device that includes "an input device for accepting a set or a plurality of sets of input information; one or a plurality of input buffers; a means for transporting the input information to the input buffer . . . one or a plurality of recording structures, referred to as a cortex . . . the output buffer being operable to transform the wave-modeled retrieval into output data; and a means for using control data to provide overall control of the associative memory device." As such, in regards to the first stated rejection under 35 U.S.C. 101, the subject matter of claim 1 **as a whole** is not a "disembodied mathematical concept representing nothing more than a 'law of nature' or an 'abstract idea,'" but rather incorporates mathematical concepts that have been "reduced to some practical application rendering [them] 'useful.'" It is simply improper, as explained by the Federal Circuit in *State Street Bank*, *Alappat*, *AT&T*, and numerous other decisions, to create an overly broad, fourth category of [mathematical] subject matter excluded from § 101. The claimed invention of claim 1 as a whole is directed toward forming a specific associative memory device that produces a useful, concrete, and tangible result of wave-modeled retrieval.

Likewise, in regards to the second stated grounds for rejection under 35 U.S.C. 101, the Title is cited to support the conclusion that "[w]aves are synonymous with signals and signals are non-statutory." Not only does rejecting the claims based on the Title fail to comply with the mandate of M.P.E.P. 2107.02 that each claim must be evaluated on its own merits, it defies credulity to suggest that systems that process signals, such as radios, televisions, telephones, radar, satellites, cameras, and numerous other items that have a readily apparent practical application are not patentable simply because they process signals, and because "signals are non-

statutory," such widely-patented systems have suddenly become unpatentable.

In regards to the third ground for rejection under 35 U.S.C. 101, the claims are drawn to associative memory devices and a method of autonomous pattern recognition, not to the mathematical formula for wave propagation. The rejection of the claims is based on an improper, overly broad, fourth category of [mathematical] subject matter excluded from § 101, resulting from the failure to examine the claims as a whole.

In regards to the fourth ground for rejection under 35 U.S.C. 101, the Examiner has not made the requisite showing that the claimed invention is undefined, accomplishes nothing if C=0 (if, in fact the claimed invention would even result in the condition that C=0), is missing a major step regarding the concept of inevitableness as allegedly admitted by the application, or that the output is independent of the input. For example, again turning to claim 1, the teachings of the specification clearly establish that a situation where C=0 is to be avoided, and is not encompassed by the claims. Furthermore, the Examiner postulates a situation where the weighting factor is infinite to render C undefined. It is clear that the claims (see, e.g., claims 12, 17, 19, and 20) are drawn to data processing equipment that would be incapable of digitally representing an infinite value. Data processing equipment stores numbers in binary form, such that an infinite number of bits would be required to represent an infinite weighting factor. As such, the rejection of the claims is based on an impossible condition.

The Examiner's analysis of "invertible" is likewise incorrect, and was based apparently on a text search for that term and not on a review of the teachings of the specification as a whole. A search of the specification for roots of the word "invertible" reveals the following passage at paragraph 0080: "Code extraction: During the identification phase, the present invention uses an inverse procedure to extract, as accurately as possible, multiple, redundant copies of the identifier code from a retrieved pattern, or IIP, to make an identification. If the file has not previously been learned by the current invention, **then no readable pattern is retrieved by the system**." (Emphasis added) Likewise, the specification states at paragraph 0252 that "Retrieval involves the recall of information and so requires an operation inverse to that for association. If association were done by adding .psi. and .phi., then recall would require subtracting .phi. from .psi.. If multiplication were used, then the inverse operation could be division." As such, the conclusion that the specification does not disclose "the **how** of identifying such invertible mathematical relation" is not a correct conclusion and is based on the failure to consider the

claims as a whole, as well as the failure to consider the teachings of the specification as a whole.

Even though the Examiner did not provide any meaningful analysis of the claims in rejecting them under 35 U.S.C. 101, thus rendering it virtually impossible to traverse such a conclusory rejection, independent claim 1 will be discussed herein to demonstrate that the Examiner has failed to provide any legitimate basis for the rejection of the claims.

Claim 1 includes an associative memory device. A "memory device" is indisputably not a disembodied mathematical concept representing nothing more than a "law of nature" or an "abstract idea," but rather is a useful machine or article of manufacture, and as such, it is clearly drawn to statutory subject matter. Each element of claim 1 is analyzed below to demonstrate that each element is drawn to statutory subject matter:

- **an input device for accepting a set or a plurality of sets of input information** – Fig. 27 shows input devices 2701a and 2701b. An "input device" is indisputably not a disembodied mathematical concept representing nothing more than a "law of nature" or an "abstract idea," but rather is a useful machine or article of manufacture, and as such, claim 1 is clearly drawn to statutory subject matter.
- **one or a plurality of input buffers** – Fig. 27 shows buffers 2702a and 2702b. A "buffer" is indisputably not a disembodied mathematical concept representing nothing more than a "law of nature" or an "abstract idea," but rather is a useful machine or article of manufacture, and as such, claim 1 is clearly drawn to statutory subject matter.
- **the input device being coupled to, or integrated into, the input buffer** – this element provides a structural limitation for the previously recited statutory subject matter elements.
- **a means for transporting the input information to the input buffer** – as discussed at paragraph [0535] of the publication of this application, "each of the modules and controllers discussed above may be implemented by an appropriate combination of software and hardware, such as application-specific integrated circuits ("ASIC"), field programmable gate arrays ("FPGAs"), other types of custom computer chips or boards or microprocessor circuitry, and/or sets of operational amplifiers ("Op-amps"), depending upon the performance, cost, and reliability requirements of each specific deployment employing an embodiment of the present invention." Thus, the structure corresponding to this means plus function element encompasses any such well known structures for

transporting the input information to the input buffer from an input device. Structures such as microprocessor circuitry are indisputably not a disembodied mathematical concept representing nothing more than a "law of nature" or an "abstract idea," but rather are useful machines or articles of manufacture, and as such, claim 1 is clearly drawn to statutory subject matter.

- **the input buffer being adapted to transform the input information into corresponding sets of complex-valued wave fields as wave-modeled input data** – as discussed above, the input buffer is clearly statutory subject matter. As such, the claimed function of the input buffer is indisputably not a disembodied mathematical concept representing nothing more than a "law of nature" or an "abstract idea," but rather is the function of a useful machine or article of manufacture, and as such, claim 1 is clearly drawn to statutory subject matter.
- **one or a plurality of recording structures, referred to as a cortex** - Fig. 27 shows cortex 103, which as described at paragraph [0535] of the publication of this application, can be a recording structure "implemented by an appropriate combination of software and hardware, such as application-specific integrated circuits ("ASIC"), field programmable gate arrays ("FPGAs"), other types of custom computer chips or boards or microprocessor circuitry, and/or sets of operational amplifiers ("Op-amps"), depending upon the performance, cost, and reliability requirements of each specific deployment employing an embodiment of the present invention." Thus, the plurality of recording structures referred to as a cortex encompasses structures such as ASICs, FPGAs, and microprocessor circuitry, which are indisputably not disembodied mathematical concepts representing nothing more than a "law of nature" or an "abstract idea," but rather are useful machines or articles of manufacture, and as such, claim 1 is clearly drawn to statutory subject matter.
- **the input buffer being further adapted to propagate the wave-modeled input data to the cortex** - as discussed above, the input buffer is clearly statutory subject matter. As such, the claimed function of the input buffer is indisputably not a disembodied mathematical concept representing nothing more than a "law of nature" or an "abstract idea," but rather is the function of a useful machine or article of manufacture, and as such, claim 1 is clearly drawn to statutory subject matter.

- **the cortex being adapted to associate the desired sets of wave-modeled input data through an invertible mathematical function or operation, thus creating one or a plurality of associations within the cortex** - as discussed above, the cortex is clearly statutory subject matter. As such, the claimed function of the cortex is indisputably not a disembodied mathematical concept representing nothing more than a "law of nature" or an "abstract idea," but rather is the function of a useful machine or article of manufacture, and as such, claim 1 is clearly drawn to statutory subject matter.
- **the cortex being further adapted to store the associations in a distributed manner across a cortex surface with other previously stored associations** - as discussed above, the cortex is clearly statutory subject matter. As such, the claimed function of the cortex is indisputably not a disembodied mathematical concept representing nothing more than a "law of nature" or an "abstract idea," but rather is the function of a useful machine or article of manufacture, and as such, claim 1 is clearly drawn to statutory subject matter.
- **the cortex being further adapted to form and store linear combinations of associations** - as discussed above, the cortex is clearly statutory subject matter. As such, the claimed function of the cortex is indisputably not a disembodied mathematical concept representing nothing more than a "law of nature" or an "abstract idea," but rather is the function of a useful machine or article of manufacture, and as such, claim 1 is clearly drawn to statutory subject matter.
- **an input device being operable to accept one or a plurality of retrieval prompts, referred to as a prompt** - as discussed above, the input device is clearly statutory subject matter. As such, the claimed function of the input device is indisputably not a disembodied mathematical concept representing nothing more than a "law of nature" or an "abstract idea," but rather is the function of a useful machine or article of manufacture, and as such, claim 1 is clearly drawn to statutory subject matter.
- **the input buffer being operable to transform the prompt into a corresponding set of complex-valued wave fields, as a wave-modeled prompt** - as discussed above, the cortex is clearly statutory subject matter. As such, the claimed function of the cortex is indisputably not a disembodied mathematical concept representing nothing more than a "law of nature" or an "abstract idea," but rather is the function of a useful machine or article of manufacture, and as such, claim 1 is clearly drawn to statutory subject matter.

- **the input buffer being operable to propagate the wave-modeled prompt to the cortex** - as discussed above, the input buffer is clearly statutory subject matter. As such, the claimed function of the input buffer is indisputably not a disembodied mathematical concept representing nothing more than a "law of nature" or an "abstract idea," but rather is the function of a useful machine or article of manufacture, and as such, claim 1 is clearly drawn to statutory subject matter.
- **the cortex being operable to cause the wave-modeled prompt to mathematically operate upon the previously stored associations using a de-association operation that is the inverse of that originally used to form the associations** - as discussed above, the cortex is clearly statutory subject matter. As such, the claimed function of the cortex is indisputably not a disembodied mathematical concept representing nothing more than a "law of nature" or an "abstract idea," but rather is the function of a useful machine or article of manufacture, and as such, claim 1 is clearly drawn to statutory subject matter.
- **the cortex being adapted to store the wave-modeled prompt with other previously stored associations and wave modeled prompts** - as discussed above, the cortex is clearly statutory subject matter. As such, the claimed function of the cortex is indisputably not a disembodied mathematical concept representing nothing more than a "law of nature" or an "abstract idea," but rather is the function of a useful machine or article of manufacture, and as such, claim 1 is clearly drawn to statutory subject matter.
- **a means for the result of the mathematical de-association operation, representing a wave-modeled retrieval, to propagate from the cortex to one or a plurality of output buffers, said output buffer being referred to with the input buffer as the buffers** – as discussed at paragraph [0535] of the publication of this application, "each of the modules and controllers discussed above may be implemented by an appropriate combination of software and hardware, such as application-specific integrated circuits ("ASIC"), field programmable gate arrays ("FPGAs"), other types of custom computer chips or boards or microprocessor circuitry, and/or sets of operational amplifiers ("Op-amps"), depending upon the performance, cost, and reliability requirements of each specific deployment employing an embodiment of the present invention." Thus, the structure corresponding to this means plus function element encompasses any such well known structures for

transporting the claimed information from the cortex to one or a plurality of output buffers. Structures such as microprocessor circuitry are indisputably not a disembodied mathematical concept representing nothing more than a "law of nature" or an "abstract idea," but rather are useful machines or articles of manufacture, and as such, claim 1 is clearly drawn to statutory subject matter.

- **the output buffer being operable to transform the wave-modeled retrieval into output data** - as discussed above, the buffers are clearly statutory subject matter. As such, the claimed function of the buffers is indisputably not a disembodied mathematical concept representing nothing more than a "law of nature" or an "abstract idea," but rather is the function of a useful machine or article of manufacture, and as such, claim 1 is clearly drawn to statutory subject matter.
- **a means for using control data to provide overall control of the associative memory device** – as discussed at paragraph [0535] of the publication of this application, "each of the modules and controllers discussed above may be implemented by an appropriate combination of software and hardware, such as application-specific integrated circuits ("ASIC"), field programmable gate arrays ("FPGAs"), other types of custom computer chips or boards or microprocessor circuitry, and/or sets of operational amplifiers ("Op-amps"), depending upon the performance, cost, and reliability requirements of each specific deployment employing an embodiment of the present invention." Thus, the structure corresponding to this means plus function element encompasses any such well known structures for using control data to provide overall control of a memory device. Structures such as microprocessor circuitry are indisputably not a disembodied mathematical concept representing nothing more than a "law of nature" or an "abstract idea," but rather are useful machines or articles of manufacture, and as such, claim 1 is clearly drawn to statutory subject matter.

Thus, the Applicant has demonstrated in painstaking detail that claim 1 is not an attempt "to patent the mathematical formula for wave propagation," as asserted by the Examiner at paragraph 11 of the Final Office Action mailed November 22, 2006, but rather includes mathematical concepts that have been reduced to a practical application, rendering them useful. The Examiner's utter failure to even attempt to address the factors set forth by the Federal Circuit in *In re Alappat* and related cases in regards to the claimed subject matter and the

Examiner's reliance on the specification and title as a basis for the rejection merely underscores the fact that the Examiner has failed to apply the proper legal standards in rejecting claim 1 under 35 U.S.C. 101, and must therefore be **REVERSED**.

While a similar analysis of independent claims 38 and 74 and all dependent claims could likewise be performed, the detailed analysis above has clearly shown that the Examiner's conclusory and legally improper basis for rejecting all of the claims is baseless. The Applicant reserves the right to further demonstrate that all pending claims are drawn to statutory subject matter, at least for the reasons set forth above. The rejection of the claims under all stated bases of 35 U.S.C. 101 must therefore be **REVERSED.**

4. Whether the Examiner has properly rejected the claims under 35 U.S.C. 101 for lacking utility.

In regards to the first rejection of the claims under 35 U.S.C. 112, it is stated that the rejection was only applied because of the rejection of the claims under 35 U.S.C. 101. As that rejection is improper, withdrawal of the rejection of the claims under the first stated basis of 35 U.S.C. 112 is respectfully requested.

VIII. APPENDIX OF CLAIMS (37 C.F.R. § 41.37(c)(8))

The text of the claims involved in the appeal are as follows:

1. An associative memory device, comprising:

an input device for accepting a set or a plurality of sets of input information;

one or a plurality of input buffers;

the input device being coupled to, or integrated into, the input buffer;

a means for transporting the input information to the input buffer;

the input buffer being adapted to transform the input information into corresponding sets of complex-valued wave fields as wave-modeled input data;

one or a plurality of recording structures, referred to as a cortex;

the input buffer being further adapted to propagate the wave-modeled input data to the cortex;

the cortex being adapted to associate the desired sets of wave-modeled input data through an invertible mathematical function or operation, thus creating one or a plurality of associations within the cortex;

the cortex being further adapted to store the associations in a distributed manner across a cortex surface with other previously stored associations;

the cortex being further adapted to form and store linear combinations of associations;

an input device being operable to accept one or a plurality of retrieval prompts, referred to as a prompt;

the input buffer being operable to transform the prompt into a corresponding set of complex-valued wave fields, as a wave-modeled prompt;

the input buffer being operable to propagate the wave-modeled prompt to the cortex;

the cortex being operable to cause the wave-modeled prompt to mathematically operate upon the previously stored associations using a de-association operation that is the inverse of that originally used to form the associations;

the cortex being adapted to store the wave-modeled prompt with other previously stored associations and wave modeled prompts;

a means for the result of the mathematical de-association operation, representing a wave-modeled retrieval, to propagate from the cortex to one or a plurality of output buffers, said output buffer being referred to with the input buffer as the buffers;

the output buffer being operable to transform the wave-modeled retrieval into output data; and

a means for using control data to provide overall control of the associative memory device.

2. The associative memory device of Claim 1, wherein the input device further comprises a module for pre-processing the input information.

3. The associative memory device of Claim 2, wherein the pre-processing module is adapted to assign phase information to the input information.

4. The associative memory device of Claim 1, further comprising a module for performing post-processing on the wave-modeled retrieval or output data.

5. The associative memory device of Claim 1, further comprising a means for exporting the wave-modeled retrieval or output data to one or more output devices.

6. The associative memory device of Claim 1, further comprising a means for retaining input information, wave-modeled input data, prompts, wave modeled prompts, wave modeled retrieval and output data in a volatile memory structure.

7. The associative memory device of Claim 1, further comprising a means for processing the input information, wave-modeled input data, prompt, wave-modeled prompt, wave-modeled retrieval, output data or control data.

8. The associative memory device of Claim 1 further comprising a permanent storage device for saving the input information, wave-modeled input data, prompt, wave-modeled prompt, wave-modeled retrieval, output data or control data.

9. The associative memory device of Claim 1, wherein physical or electronic stimuli comprise the input information.

10. The associative memory device of Claim 9, wherein the physical or electronic stimuli that are processed further comprises images, fingerprints, signatures, faces, sounds, gas molecules, liquids or chemical compositions.

11. The associative memory device of Claim 9, wherein a sensor or plurality of sensors are operable to accept the physical or electronic stimuli.

12. The associative memory device of Claim 11, wherein the sensors further comprise a camera, scanner, keyboard, computer, mouse, analog recorder, digital recorder, odor detector, digital signature capture apparatus, or microphone.

13. The associative memory device of Claim 1, wherein the input buffer is operable to:

transform input information into corresponding sets of complex-valued wave fields;

transform prompts into corresponding sets of complex-valued wave fields;

propagate wave-modeled input data to the cortex; and

propagate wave-modeled prompts to the cortex.

14. The associative memory device of Claim 1, wherein output buffer is operable to:

accept the wave-modeled retrieval propagated from the cortex;

transform the wave-modeled retrieval from a complex-valued wave fields to a data format.

15. The associative memory device of Claim 1, wherein the input buffer and the output buffer further comprise a single buffer unit adapted to operate in either an input mode, an output mode, or both simultaneously.

16. The associative memory device of Claim 1, wherein the cortex further comprises a plurality of interconnected modules to perform associated memory operations further comprising:

a module to receive and store sets of complex-valued wave fields propagated from the

input buffer;

a second module to form and store associations with propagated wave fields using an invertible mathematical operation;

a module to form and store linear combinations of associations;

a module to receive a wave-modeled prompt;

a module to mathematically operate upon the previously stored associations using a de-association function that is the inverse of that originally used to form the associations;

a module to generate the complex conjugate of the de-associated wave fields; and

a module to propagate the results of the operation to the output buffer.

17. The associative memory device of Claim 1, wherein the buffers further comprise:

physical antenna arrays;

computer hardware which is coupled to the physical antenna arrays; and

computer software being adapted to program the computer hardware to perform wave modeling, wave propagation, wave reception and wave transformation operations.

18. The associative memory device of Claim 17, wherein the physical antenna arrays further comprise:

multiple receiving antennas with corresponding receiver memory elements;

multiple broadcast antennas with corresponding broadcast memory elements;

a receiver array controller; and

a broadcast array controller.

19. The associative memory device of Claim 17, wherein the computer hardware further comprises;

an analog-to-digital converter with an input and output;

a device driver coupled to the input of the analog-to-digital converter;

a preprocessor module with an input and output;

the input to the preprocessor module coupled to the output of the analog-to-digital converter;

a phase assignment module with an input and an output;

the output of the preprocessor module coupled to an input of the phase assignment module;

a central processing unit (CPU);

the CPU having a main buffer memory;

the output of the phase assignment module being coupled to or integral to the CPU;

a post-processor module with an input and output; and

the CPU being coupled to the input of the post-processor module.

20. The associative memory device of Claim 1, wherein the buffer further comprises:

computer hardware with an input and output;

computer software adapted to program the computer hardware;

a device driver, with an input and an output,

the output of the device driver being coupled to the input of the computer hardware;

an analog-to-digital converter being integral to the computer hardware operable to convert analog input information into digital input information;

a pre-processor module, the pre-processor module being integral to the computer hardware or configured therein with the computer software and being operable to process input information;

a phase assignment module, the phase assignment module being integral to the computer hardware or configured therein with the computer software, and being operable for conditioning the input information into wave-modeled input data;

a post-processor module, the post-processor module being integral to the computer hardware or configured therein with the computer software and being operable to transform the wave-modeled retrieval into output data;

a wave propagation calculation module, the wave propagation calculation module being integral to the computer hardware or configured therein with the computer software and being operable to calculate wave propagation properties;

the computer hardware having a main buffer memory for storing the input information, wave-modeled input data, prompt, wave-modeled prompt, wave-modeled retrieval, output data or control data; and

buffer data arrays comprising both receiver memory elements and broadcast memory

elements being integral to the computer hardware.

21. The associative memory device of Claim 1, wherein the buffers further comprise:

an application-specific integrated circuit (ASIC) or a field programmable gate array (FPGA) with an input and output;

a device driver, with an input and an output,

the output of the device driver being coupled to the input of the ASIC or FPGA;

an analog-to-digital converter being integral or external to the ASIC or FPGA operable to convert analog input information into digital input information,

a pre-processor module, the pre-processor module being integral or external to the ASIC or FPGA and being operable to process input information;

a phase assignment module, the phase assignment module being integral or external to the ASIC or FPGA and being operable to condition the input information into wave-modeled input data;

a post-processor module, the post-processor module being integral or external to the ASIC or FPGA and being operable to transform the wave-modeled retrieval into output data;

a wave propagation calculation module, the wave propagation calculation module being integral or external to the ASIC or FPGA and being operable to calculate wave propagation properties;

the ASIC or FPGA having a main buffer memory for storing the input information, wave-modeled input data, prompt, wave-modeled prompt, wave-modeled retrieval, output data or control data; and

buffer data arrays comprising both receiver memory elements and broadcast memory elements being integral or external to the ASIC or FPGA.

22. The associative memory device of Claim 1, wherein the buffers further comprise:

an analog computer system utilizing a plurality of operational amplifiers, said analog computer having an input and output;

a device driver, with an input and an output;

the output of the device driver being coupled to the input of the analog computer;

a pre-processor module, the pre-processor module being integral or external to the analog

computer and being operable to process input information;

a phase assignment module, the phase assignment module being integral or external to the analog computer and being operable to condition the input information into wave-modeled input data;

a post-processor module, the post-processor module being integral or external to the analog computer and being operable to transform the wave-modeled retrieval into output data;

a wave propagation calculation module, the wave propagation calculation module being integral or external to the analog computer and being operable to calculate wave propagation properties;

the analog computer having a main buffer memory for storing the input information, wave-modeled input data, prompt, wave-modeled prompt, wave-modeled retrieval, output data or control data; and

buffer data arrays comprising both receiver memory elements and broadcast memory elements being integral to the analog computer.

23. The associative memory device of Claim 1, wherein the cortex further comprises:

a physical antenna array;

a processing unit with an input and output;

the physical antenna array being coupled to the input of the processing unit;

the physical antenna array having a receiver array controller, a broadcast array controller, multiple receiving antennas with corresponding receiver memory elements, one set of receiver memory elements for each buffer element in the associative memory device, and multiple broadcast antennas with corresponding broadcast memory elements;

an association module, the association module being integral to the processing unit;

a de-association module, the de-association module being integral to the processing unit;

a linear combination module, the linear combination module being integral to the processing unit;

a complex conjugation module, the complex conjugation module being integral to the processing unit;

a main cortex memory being integral to the processing unit, the main cortex memory further comprising association memory elements; de-association memory elements; and linear

combination memory elements.

24. The associative memory device of Claim 23, wherein the cortex further comprises:

a wave propagation calculation module, the wave propagation calculation module being integral to the processing unit and being operable to calculate wave propagation properties; and

cortex data arrays comprised of receiver memory elements, one set of receiver memory elements for each buffer in the associative memory system, broadcast memory elements, association memory elements, de-association memory elements, and linear combination memory elements.

25. The associative memory device of Claim 23, wherein the processing unit further comprises a programmable computer hardware and computer software system, an application-specific integrated circuit (ASIC) or a field programmable gate array (FPGA).

26. The associative memory device of Claim 23, wherein the processing unit further comprises an analog computer system utilizing a plurality of operational amplifiers.

27. The associative memory device of Claim 23, wherein the processing unit further comprises a programmable computer hardware and computer software system, an application-specific integrated circuit (ASIC) a field programmable gate array (FPGA) or an analog computer system utilizing a plurality of operational amplifiers.

28. The associative memory device of Claim 1, wherein the implementation of the associative memory device is mathematically modeled with wave-modeled input data on the buffer being denoted by:

$P_i, P_j, \ldots, P_l$;

the propagated forms of the wave-modeled input data on the cortex being denoted by:

$P_i', P_j', \ldots, P_l'$;

an association formed from the wave-modeled input data being denoted by:

$\langle P_i', P_j', \ldots, P_l' \rangle \equiv f(P_i', P_j', \ldots, P_l')$,

in which the association operation is defined by an invertible mathematical function f and a linear combination of associations being denoted by:

$$\sum_m \alpha_m \langle \acute{P}_{i,m}, \acute{P}_{j,m}, \ldots, \acute{P}_{l,m} \rangle = \sum_m \alpha_m f(\acute{P}_{i,m}, \acute{P}_{j,m}, \ldots \acute{P}_{l,m}),$$

where α_m is a weighting factor for the m^{th} association.

29. The associative memory device of Claim 28, wherein the association function f corresponds to the mathematical operation of multiplication such that two propagated input patterns $\acute{P}_i = \psi_m$ and $\acute{P}_j = \phi_m$ are associated by multiplying the complex amplitudes of the two wave functions, point by point, at each location $\mathbf{r}_C$ in the cortex, with the association represented mathematically as:

$$\psi_m(\mathbf{r}_C)\phi_m(\mathbf{r}_C)$$

and with all associations previously stored, C, written as the linear combination of associations:

$$C(\mathbf{r}_C) = \sum_m \alpha_m \psi_m(\mathbf{r}_C)\phi_m(\mathbf{r}_C).$$

30. The associative memory device of Claim 28, wherein the association function f corresponds to the mathematical operation of multiplication of wave fields, one or more of which may be point-wise normalized, the rest non-normalized, such that two propagated input patterns $\acute{P}_i = \psi_m$ and $\acute{P}_j = \phi_m$ are associated by multiplying the point-wise complex amplitudes of the two wave functions, at each location $\mathbf{r}_C$ in the cortex with the association represented mathematically as:

$$\exp[i\,Arg(\psi(\mathbf{r}_C))]\exp[i\,Arg(\phi(\mathbf{r}_C))]$$

or

$$\psi(\mathbf{r}_C)\exp[i\,Arg(\phi(\mathbf{r}_C))]$$

where Arg(z) is the phase angle for a complex value z, and with all associations previously stored written as the linear combination of associations:

$$C(\mathbf{r}_C) = \sum_m \alpha_m \exp[i\,Arg(\psi_m(\mathbf{r}_C))]\exp[i\,Arg(\phi_m(\mathbf{r}_C))]$$

or

$$C(\mathbf{r}_C) = \sum_m \alpha_m \psi_m(\mathbf{r}_C)\exp[i\,Arg(\phi_m(\mathbf{r}_C))]$$

31. The associative memory device of Claim 1, wherein the implementation of the associative memory device is mathematically modeled with the wave-modeled prompt on the input buffer being denoted by:

$R_i, R_j, \ldots, R_l$;

the respective propagated forms of the wave-modeled prompt on the cortex being denoted by:

$R_i', R_j', \ldots, R_l'$,

the wave-modeled prompt being operable to probe the plurality of previously stored associations using f^{-1}, the inverse of the function used originally to form the associations; and

the resulting de-associated wave D' being denoted by:

$$D' = \langle C \mid R_i', R_j', \ldots, R_l' \rangle = f^{-1}(C \mid R_i', R_j', \ldots, R_l') = f^{-1}\left(\sum_m \alpha_m f(P_{i,m}', P_{j,m}', \ldots P_{l,m}') \mid R_i', R_j', \ldots, R_l'\right);$$

where α_m is a weighting factor for the m^{th} association, a de-association is denoted by angle brackets with a vertical bar separating the first argument, the entity being probed, from the second argument, the set of one or more prompting fields; and D represents the retrieval formed when the complex conjugate of the de-association (D'^*) is propagated from the cortex to the output buffer.

32. The associative memory device of Claim 31 further comprising multiplication for the association operation, and the inverse function, f^{-1}, division for the retrieval operation, wherein if a wave field ϕ_n is used to probe the previously stored associated pairs in the cortex, then the retrieval process is denoted by:

$$\mathbf{C}\phi_n = \sum_m \alpha_m \psi_m \phi_m \mathbf{I} \phi_n = \sum_m \alpha_m \psi_m \phi_m \phi_n^{-1} = \alpha_n \psi_n + \sum_{m \neq n} \alpha_m \psi_m \phi_m \phi_n^{-1},$$

further, given that the inverse operator **I** corresponds to division, the retrieval process is more specifically denoted by:

$$\mathbf{C}\phi_n = \sum_m \frac{\alpha_m \psi_m \phi_m}{\phi_n} = \alpha_n \psi_n + \sum_{m \neq n} \frac{\alpha_m \psi_m \phi_m}{\phi_n}$$

where **C** contains the linear combination of previously stored associations, and, at each point on the cortex $\mathbf{r}_c$ on which **C** is defined, the value of **C** is divided by the value of ϕ_n, with the

retrieval, $\alpha_n \psi_n$, being propagated to the output buffer and then to the output device.

33. The associative memory device of Claim 30, further comprising:

a retrieval operation, multiplication corresponding to the association operation, using complex conjugation as the inverse function f^{-1}, such that if the point-wise normalized wave field ϕ_n is used to probe the previously stored associated pairs in the cortex;

the probe process being denoted by:

$$\mathbf{C}\phi_n = \sum_m \alpha_m \exp[i\mathrm{Arg}(\psi_m)]\exp[i\mathrm{Arg}(\phi_m)]\mathbf{I}\exp[i\mathrm{Arg}(\phi_n)]$$
$$= \sum_m \alpha_m \exp[i\mathrm{Arg}(\psi_m)]\exp[i\mathrm{Arg}(\phi_m)]\exp[i\mathrm{Arg}(\phi_n)]^{-1}$$

or

$$\mathbf{C}\phi_n = \sum_m \alpha_m \psi_m \exp[i\mathrm{Arg}(\phi_m)]\mathbf{I}\exp[i\mathrm{Arg}(\phi_n)] = \sum_m \alpha_m \psi_m \exp[i\mathrm{Arg}(\phi_m)]\exp[i\mathrm{Arg}(\phi_n)]^{-1}$$

further, given that the inverse operator **I**, which embodies the inverse function f^{-1}, corresponds to complex conjugation, the probe process more specifically by:

$$\mathbf{C}\phi_n = \sum_m \alpha_m \exp[i\mathrm{Arg}(\psi_m)]\exp[i\mathrm{Arg}(\phi_m)]\exp[-i\mathrm{Arg}(\phi_n)]$$
$$= \alpha_n \exp[i\mathrm{Arg}(\psi_n)] + \sum_{m\neq n} \alpha_m \exp(i[\mathrm{Arg}(\psi_m) + \mathrm{Arg}(\phi_m) - \mathrm{Arg}(\phi_n)])$$

or

$$\mathbf{C}\phi_n = \sum_m \alpha_m \psi_m \exp[i\mathrm{Arg}(\phi_m)]\exp[-i\mathrm{Arg}(\phi_n)]$$
$$= \alpha_n \psi_n + \sum_{m\neq n} \alpha_m \psi_m \exp(i[\mathrm{Arg}(\phi_m) - \mathrm{Arg}(\phi_n)])$$

where **C** contains the linear combination of previously stored associations, and, at each point $\mathbf{r}_c$ on the cortex on which **C** is defined, the value of **C** is multiplied by the complex conjugate of the exponential of the phase angle of the prompt ϕ_n, with the retrieval being propagated to the output buffer and to the output device.

34. The associative memory device of Claim 1, wherein the means of transport of input information, a prompt and a retrieval is through the propagation of physical waves by antenna arrays and supporting computer hardware and computer software.

35. The associative memory device of Claim 1, further comprising computer hardware and computer software operable to transport input information, prompt and retrieval through the simulation of wave propagation in which sets of data representing input information, prompt and retrieval are input, pre-processed, and then represented as wave functions $\xi_i(\mathbf{r})$ that are time-harmonic solutions to the wave equation:

$$\left(\nabla^2 + k^2\right)\xi_i(\mathbf{r}) = 0;$$

in which the propagation of a wave away from a surface (for example, a buffer or a cortex) is formally and exactly described by the Kirchhoff integral:

$$\xi_i(\mathbf{r}) = \oiint_{S_C} d\mathbf{S}_C \cdot \{\xi_i(\mathbf{r}_C)\nabla_C G(\mathbf{r},\mathbf{r}_C) - G(\mathbf{r},\mathbf{r}_C)\nabla_C \xi_i(\mathbf{r}_C)\}$$

where the surface S_C is closed and completely surrounds a destination point $\mathbf{r}$, the gradient operates only on coordinates on the source surface S_C, and $G(\mathbf{r},\mathbf{r}_C)$ is a Green's function; and in which the above continuous integral is discretized for numerical implementation as:

$$\xi(\mathbf{r}) = \sum_{\text{all source points}} \Delta\mathbf{S}_C \cdot \{\xi(\mathbf{r}_C)\nabla_C G(\mathbf{r},\mathbf{r}_C) - G(\mathbf{r},\mathbf{r}_C)\nabla_C \xi(\mathbf{r}_C)\}$$

thus enabling digital input, output, and computation.

36. The associative memory device of Claim 35, wherein said computer hardware and computer software comprises a combination of hardwired wave propagation circuitry and software running on computer hardware.

37. The associative memory device of Claim 1, wherein the wave-modeled retrieval and output data corresponds to any of the sets of wave-modeled input data propagated to the cortex and associated with other data.

38. An associative memory device, comprising:

one or a plurality of input devices;

one or a plurality of input buffers;

one or a plurality of recording structures, referred to as a cortex;

one or a plurality of output buffers, referred to with the input buffer as the buffers;

one or a plurality of output devices;

one or a plurality of overall system controllers;

one or a plurality of volatile memory units;

one or a plurality of permanent storage devices, and one or a plurality of processing units;

the input device operable to sense input information comprising physical or electronic stimuli;

the input device being coupled to the input buffer and being further operable to transport the input information to the input buffer;

the input buffer operable to transform the input information into corresponding sets of complex-valued wave fields;

the input buffer being further operable to pre-process the input information and assign phase information;

the input buffer being further operable to propagate the sets of complex-valued wave fields representing the input information and referred to as wave-modeled input data to the cortex;

the cortex being operable to accept the wave-modeled input data;

the cortex being adapted to retain the wave-modeled input data from the input buffer in a distributed manner across a cortex surface;

the cortex being further operable to associate the desired sets of wave-modeled input data through an invertible mathematical function or operation, thus creating one or more associations within the cortex;

the cortex being further operable to create and store linear combinations of associations;

the input device, when enabled, being further operable to sense additional sets of input information comprising physical or electronic stimuli or other input data to act as a prompt or prompts to make a retrieval or retrievals;

the input buffer being further operable to transform the prompting set of input information into corresponding sets of complex-valued wave fields, referred to as the wave-modeled prompt;

the input buffer being further operable to preprocess the prompting set of input information and assign phase information;

the input information to be retrieved from the cortex comprising any of the sets of physical or electronic stimuli stored in previously created associations, as determined by the operator;

the input buffer, when enabled, being further operable to propagate the wave-modeled prompt to the cortex;

the cortex being operable to accept a probe from the input buffer carried by a wave-modeled prompt using a de-association function or operation that is the inverse of that originally used to form the association;

the cortex being further operable to propagate the results of the de-association, representing a retrieval, to the output buffer;

the output buffer being adapted to receive, post-process, and export the retrieval to one or more output devices in human or machine-readable form.

39. The associative memory device of Claim 38, the buffer and cortex are operable to generate and propagate wave fronts within the associative memory device.

40. The associative memory device of Claim 38, wherein a first set of buffers processes images, a second set of buffers processes sounds, a third set of buffers processes representations of gas molecules and a fourth set of buffers processes chemical compositions.

41. The associative memory device of Claim 38, wherein the cortex is adapted to store a plurality of sensed physical or electronic data in a distributed manner.

42. The associative memory device of Claim 38, wherein the input buffer, cortex and output buffer are adapted to receive and process a plurality of sensed physical or electronic stimuli simultaneously.

43. The associative memory device of Claim 38, adapted to perform autonomous pattern recognition or identification operations.

44. The associative memory device of Claim 43, further comprising:

an internal identification pattern (IIP) buffer, operable to store unique, machine-readable patterns for autonomous identification purposes;

an IIP generator module, operable to create a unique, machine-readable pattern given a

unique identification code chosen automatically or supplied by a system operator;

the IIP generator module, further operable to link each specific IIP to sets of information (such as data files) to be recalled, sets of commands to be executed or communicated upon a positive identification, and threshold confidence levels required for execution of each particular command or sets of commands;

an IIP reader module, operable to read autonomously a retrieved pattern and deduce an identification code that corresponds to a previously created IIP;

the IIP reader module further operable to provide a confidence estimate based on relative certainty or uncertainty of its identification;

an autonomous execution module, operable to receive the identification result and confidence estimate from the IIP reader module, to recall the associated files or other information related to the reported identification code, and further to execute or communicate the appropriate commands based on the identification code, the reported confidence estimate, and the predefined confidence levels required for the relevant commands;

an adaptive learning module, operable to modify the plurality of associations stored in the cortex in response to feedback on the accuracy of its identification, so as to improve its recognition performance, in which the general adaptation process is defined by the following equation for the case of a false positive identification of prompting pattern R_i:

$C_{new} = C_{old} - \beta_i \langle R_i, I_j \rangle$

where C_{old} is the original cortex value, C_{new} is the cortex value after adaptive learning, β_i is a positive weighting factor, and I_j is the incorrectly retrieved IIP;

and where the general adaptation process is defined by the following equation for the case of a false negative or overly weak positive identification of prompting pattern R_i:

$$C_{new} = C_{old} + \beta_i \langle R_i - \gamma_i P_i, I_i \rangle$$

where C_{old} is the original cortex value, C_{new} is the cortex value after adaptive learning, β_i is a positive weighting factor, I_i is the desired IIP, P_i is the original pattern associated with I_i, and γ_i is 0 for augmentation mode and 1 for replacement mode.

45. The associative memory device of Claim 44, further comprising computer hardware and software.

46. The associative memory device of Claim 44, further comprising one or a plurality of application-specific integrated circuits (ASICs) or field programmable gate arrays (FPGAs).

47. The associative memory device of Claim 44 further comprising an analog computer system utilizing a plurality of operational amplifiers.

48. The associative memory device of Claim 44, wherein the pattern recognized is an image, human face, fingerprint, signature, gas molecule, substance, liquid or chemical composition.

49. The associative memory device of Claim 43, wherein a sensor or plurality of sensors comprise the input device.

50. The associative memory device of Claim 49, wherein the sensor comprises a film still or moving picture camera, still or moving video camera, scanner, a device to convert gas molecules into signals, or a microphone.

51. The associative memory device of Claim 50, wherein the device to convert gas molecules into signals comprises directly heated short chromatography columns, cooled sample traps, surface acoustic wave (SAW) interferometric vapor detectors.

52. The associative memory device of Claim 43, wherein the input data representing physical stimuli comprises analog or discrete electrical signals .

53. The associative memory device of Claim 43, wherein the means of information transport is through the propagation of physical waves by antenna arrays and supporting hardware and software.

54. The associative memory device of Claim 43, wherein the means of information transport is through the simulation of wave propagation in computer software operating on computer hardware, in which sets of data are input, pre-processed, and then represented as wave

functions $\xi_i(\mathbf{r})$ that are time-harmonic solutions to the wave equation:

$$\left(\nabla^2 + k^2\right)\xi_i(\mathbf{r}) = 0;$$

in which the propagation of a wave away from a surface such as a buffer or the cortex is formally and exactly described by the Kirchhoff integral:

$$\xi_i(\mathbf{r}) = \oiint_{S_C} d\mathbf{S}_C \cdot \{\xi_i(\mathbf{r}_C)\nabla_C G(\mathbf{r},\mathbf{r}_C) - G(\mathbf{r},\mathbf{r}_C)\nabla_C \xi_i(\mathbf{r}_C)\}$$

where the surface S_C is closed and completely surrounds a destination point $\mathbf{r}$, the gradient operates only on coordinates on the source surface S_C, and $G(\mathbf{r},\mathbf{r}_C)$ is a Green's function; and in which the above continuous integral is discretized for numerical implementation as

$$\xi(\mathbf{r}) = \sum_{\text{all source points}} \Delta\mathbf{S}_C \cdot \{\xi(\mathbf{r}_C)\nabla_C G(\mathbf{r},\mathbf{r}_C) - G(\mathbf{r},\mathbf{r}_C)\nabla_C \xi(\mathbf{r}_C)\}$$

thus enabling digital input, output, and computation.

55. The associative memory device of Claim 43, wherein said computer hardware and computer software comprises a combination of hardwired wave propagation circuitry and software running on computer hardware.

56. The associative memory device of Claim 43, wherein the wave-modeled retrieval and output data corresponds to any of the sets of wave-modeled input data propagated to the cortex and associated with other data.

57. The associative memory device of Claim 43, wherein the buffers further comprise:

physical antenna arrays;

computer hardware which is coupled to the physical antenna arrays; and

computer software being adapted to program the computer hardware to perform wave modeling, wave propagation, wave reception and wave transformation operations.

58. The associative memory device of Claim 57, wherein the physical antenna arrays further comprise:

multiple receiving antennas with corresponding receiver memory elements;

multiple broadcast antennas with corresponding broadcast memory elements;

a receiver array controller; and

a broadcast array controller.

59. The associative memory device of Claim 57, wherein the computer hardware further comprises:

an analog-to-digital converter with an input and output;

a device driver coupled to the input of the analog-to-digital converter;

a preprocessor module with an input and output;

the input to the preprocessor module coupled to the output of the analog-to-digital converter;

a phase assignment module with an input and an output;

the output of the preprocessor module coupled to an input of the phase assignment module;

a central processing unit (CPU);

the CPU having a main buffer memory;

the output of the phase assignment module being coupled to or integral to the CPU;

a post-processor module with an input and output; and

the CPU being coupled to the input of the post-processor module.

60. The buffers of Claim 43, further comprising:

computer hardware with an input and output;

computer software adapted to program the computer hardware;

a device driver, with an input and an output,

the output of the device driver being coupled to the input of the computer hardware;

an analog-to-digital converter being integral to the computer hardware operable to convert analog input information into digital input information,

a pre-processor module, the pre-processor module being integral to the computer hardware or configured therein with the computer software and being operable to process input information;

a phase assignment module, the phase assignment module being integral to the computer hardware or configured therein with the computer software, and being operable for conditioning

the input information into wave-modeled input data;

a post-processor module, the post-processor module being integral to the computer hardware or configured therein with the computer software and being operable to transform the wave-modeled retrieval into output data;

a wave propagation calculation module, the wave propagation calculation module being integral to the computer hardware or configured therein with the computer software and being operable to perform wave propagation calculations;

the computer hardware having a main buffer memory for storing the input information, wave-modeled input data, prompt, wave-modeled prompt, wave-modeled retrieval, output data or control data; and

buffer data arrays comprising both receiver memory elements and broadcast memory elements being integral to the computer hardware.

61. The associative memory device of Claim 43, wherein the buffers further comprise:

an application-specific integrated circuit (ASIC) or a field programmable gate array (FPGA) with an input and output;

a device driver, with an input and an output,

the output of the device driver being coupled to the input of the ASIC or FPGA;

an analog-to-digital converter being integral or external to the ASIC or FPGA operable to convert analog input information into digital input information,

a pre-processor module, the pre-processor module being integral or external to the ASIC or FPGA and being operable to process input information;

a phase assignment module, the phase assignment module being integral or external to the ASIC or FPGA and being operable to condition the input information into wave-modeled input data;

a post-processor module, the post-processor module being integral or external to the ASIC or FPGA and being operable to transform the wave-modeled retrieval into output data;

a wave propagation calculation module, the wave propagation calculation module being integral or external to the ASIC or FPGA and being operable to perform wave propagation calculations;

the ASIC or FPGA having a main buffer memory for storing the input information, wave-modeled input data, prompt, wave-modeled prompt, wave-modeled retrieval, output data or control data; and

buffer data arrays comprising both receiver memory elements and broadcast memory elements being integral or external to the ASIC or FPGA.

62. The associative memory device of Claim 43, wherein the buffers further comprise:

an analog computer system utilizing a plurality of operational amplifiers, said analog computer having an input and output;

a device driver, with an input and an output;

the output of the device driver being coupled to the input of the analog computer;

a pre-processor module, the pre-processor module being integral or external to the analog computer and being operable to process input information;

a phase assignment module, the phase assignment module being integral or external to the analog computer and being operable to condition the input information into wave-modeled input data;

a post-processor module, the post-processor module being integral or external to the analog computer and being operable to transform the wave-modeled retrieval into output data;

a wave propagation calculation module, the wave propagation calculation module being integral or external to the analog computer and being operable to perform wave propagation calculations;

the analog computer having a main buffer memory for storing the input information, wave-modeled input data, prompt, wave-modeled prompt, wave-modeled retrieval, output data or control data; and

buffer data arrays comprising both receiver memory elements and broadcast memory elements being integral to the analog computer.

63. The cortex of Claim 43, further comprising:

a physical antenna array;

a processing unit with an input and output;

the physical antenna array being coupled to the input of the processing unit;

the physical antenna array having a receiver array controller, a broadcast array controller, multiple receiving antennas with corresponding receiver memory elements, one set of receiver memory elements for each buffer element in the associative memory device, and multiple broadcast antennas with corresponding broadcast memory elements;

an association module, the association module being integral to the processing unit;

a de-association module, the de-association module being integral to the processing unit;

a linear combination module, the linear combination module being integral to the processing unit;

a complex conjugation module, the complex conjugation module being integral to the processing unit;

a main cortex memory being integral to the processing unit, the main cortex memory further comprising association memory elements; de-association memory elements; and linear combination memory elements.

64. The associative memory device of Claim 63, wherein the cortex further comprises:

a wave propagation calculation module, the wave propagation calculation module being integral to the processing unit and being operable to perform wave propagation calculations; and

cortex data arrays comprised of receiver memory elements, one set of receiver memory elements for each buffer in the associative memory system, broadcast memory elements, association memory elements, de-association memory elements, and linear combination memory elements.

65. The associative memory device of Claim 64, wherein the processing unit further comprises a programmable computer hardware and computer software system, an application-specific integrated circuit (ASIC) or a field programmable gate array (FPGA).

66. The associative memory device of Claim 64, wherein the processing unit further comprises an analog computer system utilizing a plurality of operational amplifiers.

67. The associative memory device of Claim 64, wherein the processing unit further comprises a programmable computer hardware and computer software system, an application-specific integrated circuit (ASIC) a field programmable gate array (FPGA) or an analog computer system utilizing a plurality of operational amplifiers.

68. The associative memory device of Claim 43, wherein the implementation of the associative memory device is mathematically modeled with wave-modeled input data on the buffer being denoted by:

$P_i, P_j, \ldots, P_l;$

the propagated forms of the wave-modeled input data on the cortex being denoted by:

$P_i', P_j', \ldots, P_l';$

an association formed from the wave-modeled input data being denoted by:

$\langle P_i', P_j', \ldots, P_l' \rangle \equiv f(P_i', P_j', \ldots, P_l'),$

in which the association operation is defined by an invertible mathematical function f and a linear combination of associations being denoted by:

$$\sum_m \alpha_m \langle P_{i,m}', P_{j,m}', \ldots, P_{l,m}' \rangle = \sum_m \alpha_m f(P_{i,m}', P_{j,m}', \ldots P_{l,m}'),$$

where α_m is a weighting factor for the m^{th} association.

69. The associative memory device of Claim 43, wherein the association function f corresponds to the mathematical operation of multiplication such that two propagated input patterns $P_i'=\psi_m$ and $P_j'=\phi_m$ are associated by multiplying the complex amplitudes of the two wave functions, point by point, at each location $\mathbf{r}_C$ in the cortex, with the association represented mathematically as:

$$\psi_m(\mathbf{r}_C)\phi_m(\mathbf{r}_C)$$

and with all associations previously stored, C, written as the linear combination of associations:

$$C(\mathbf{r}_C) = \sum_m \alpha_m \psi_m(\mathbf{r}_C)\phi_m(\mathbf{r}_C).$$

70. The associative memory device of Claim 69, wherein the association function f corresponds to the mathematical operation of multiplication of wave fields, one or more of which may be point-wise normalized, the rest non-normalized, such that two propagated input patterns

$P_i' = \psi_m$ and $P_j' = \phi_m$ are associated by multiplying the point-wise complex amplitudes of the two wave functions, at each location $\mathbf{r}_C$ in the cortex with the association represented mathematically as:

$$\exp[i\,Arg(\psi(\mathbf{r}_C))]\exp[i\,Arg(\phi(\mathbf{r}_C))]$$

or

$$\psi(\mathbf{r}_C)\exp[i\,Arg(\phi(\mathbf{r}_C))]$$

where Arg(z) is the phase angle for a complex value z, and with all associations previously stored written as the linear combination of associations:

$$C(\mathbf{r}_C) = \sum_m \alpha_m \exp[i\,Arg(\psi_m(\mathbf{r}_C))]\exp[i\,Arg(\phi_m(\mathbf{r}_C))]$$

or

$$C(\mathbf{r}_C) = \sum_m \alpha_m \psi_m(\mathbf{r}_C)\exp[i\,Arg(\phi_m(\mathbf{r}_C))]$$

71. The associative memory device of Claim 43, wherein the implementation of the associative memory device is mathematically modeled with the wave-modeled prompt on the input buffer being denoted by:

$R_i, R_j, \ldots, R_l$;

the respective propagated forms of the wave-modeled prompt on the cortex being denoted by:

$R_i', R_j', \ldots, R_l'$,

the wave-modeled prompt being operable to probe the plurality of previously stored associations using f^{-1}, the inverse of the function used originally to form the associations; and the resulting de-associated wave D' being denoted by:

$$D' = \langle C \mid R_i', R_j', \ldots, R_l' \rangle = f^{-1}(C \mid R_i', R_j', \ldots, R_l') = f^{-1}\left(\sum_m \alpha_m f(P_{i,m}', P_{j,m}', \ldots P_{l,m}') \mid R_i', R_j', \ldots, R_l'\right);$$

where α_m is a weighting factor for the m^{th} association, a de-association is denoted by angle brackets with a vertical bar separating the first argument, the entity being probed, from the second argument, the set of one or more prompting fields; and D represents the retrieval formed when the complex conjugate of the de-association (D'^*) is propagated from the cortex to the output buffer.

72. The associative memory device of Claim 71 further comprising multiplication for the association operation, and the inverse function, f^{-1}, division for the retrieval operation, wherein if a wave field ϕ_n is used to probe the previously stored associated pairs in the cortex, then the retrieval process is denoted by:

$$\mathbf{C}\phi_n = \sum_m \alpha_m \psi_m \phi_m \mathbf{I} \phi_n = \sum_m \alpha_m \psi_m \phi_m \phi_n^{-1} = \alpha_n \psi_n + \sum_{m \neq n} \alpha_m \psi_m \phi_m \phi_n^{-1},$$

further, given that the inverse operator **I** corresponds to division, the retrieval process is more specifically denoted by:

$$\mathbf{C}\phi_n = \sum_m \frac{\alpha_m \psi_m \phi_m}{\phi_n} = \alpha_n \psi_n + \sum_{m \neq n} \frac{\alpha_m \psi_m \phi_m}{\phi_n}$$

where **C** contains the linear combination of previously stored associations, and, at each point on the cortex $\mathbf{r}_c$ on which **C** is defined, the value of **C** is divided by the value of ϕ_n, with the retrieval, $\alpha_n \psi_n$, being propagated to the output buffer and then to the output device.

73. The associative memory device of Claim 72, further comprising:

a retrieval operation, corresponding to the association operation, using complex conjugation as the inverse function f^{-1}, such that if the point-wise normalized wave field ϕ_n is used to probe the previously stored associated pairs in the cortex;

the probe process being denoted by:

$$\begin{aligned}\mathbf{C}\phi_n &= \sum_m \alpha_m \exp[i\mathrm{Arg}(\psi_m)]\exp[i\mathrm{Arg}(\phi_m)]\mathbf{I}\exp[i\mathrm{Arg}(\phi_n)] \\ &= \sum_m \alpha_m \exp[i\mathrm{Arg}(\psi_m)]\exp[i\mathrm{Arg}(\phi_m)]\exp[i\mathrm{Arg}(\phi_n)]^{-1}\end{aligned}$$

or

$$\mathbf{C}\phi_n = \sum_m \alpha_m \psi_m \exp[i\mathrm{Arg}(\phi_m)]\mathbf{I}\exp[i\mathrm{Arg}(\phi_n)] = \sum_m \alpha_m \psi_m \exp[i\mathrm{Arg}(\phi_m)]\exp[i\mathrm{Arg}(\phi_n)]^{-1}$$

further, given that the inverse operator **I**, which embodies the inverse function f^{-1}, corresponds to complex conjugation, the probe process more specifically by:

$$\begin{aligned}\mathbf{C}\phi_n &= \sum_m \alpha_m \exp[i\mathrm{Arg}(\psi_m)]\exp[i\mathrm{Arg}(\phi_m)]\exp[-i\mathrm{Arg}(\phi_n)] \\ &= \alpha_n \exp[i\mathrm{Arg}(\psi_n)] + \sum_{m \neq n} \alpha_m \exp(i[\mathrm{Arg}(\psi_m) + \mathrm{Arg}(\phi_m) - \mathrm{Arg}(\phi_n)])\end{aligned}$$

or

$$\mathbf{C}\phi_n = \sum_m \alpha_m \psi_m \exp[i\mathrm{Arg}(\phi_m)]\exp[-i\mathrm{Arg}(\phi_n)]$$
$$= \alpha_n \psi_n + \sum_{m \neq n} \alpha_m \psi_m \exp(i[\mathrm{Arg}(\phi_m) - \mathrm{Arg}(\phi_n)])$$

where **C** contains the linear combination of previously stored associations, and, at each point $\mathbf{r}_c$ on the cortex on which **C** is defined, the value of **C** is multiplied by the complex conjugate of the exponential of the phase angle of the prompt ϕ_n, with the retrieval being propagated to the output buffer and to the output device.

74. A method of autonomous pattern recognition, comprising:

sensing physical or electronic stimuli with a sensor;

interfacing the output of the sensor to one or a plurality of input buffers;

converting the sensed physical or electronic stimuli at the input buffer into wave-modeled input data in the form of complex-valued wave fields;

contemporaneously pre-processing the input information and assigning phase values at the input buffer;

generating a unique internal identification pattern (IIP) based on a unique identification code assigned automatically or by a system operator to each specific set of input data;

storing the IIP in one or more IIP buffers;

linking each specific IIP to sets of information such as data files to be recalled, sets of commands to be executed or communicated upon a positive identification, and threshold confidence levels required for execution of each particular command or sets of commands;

using wave propagation to transport the wave-modeled input data and IIPs from their respective buffers to one or a plurality of recording structures, referred to as a cortex;

associating the desired sets of wave-modeled input data and their respective IIPs through an invertible mathematical function or operation, thus creating one or more associations within the cortex;

retaining the associations in a distributed manner across the cortex;

creating and storing linear combinations of associations;

inputting prompting data into the input buffer;

converting the prompting data at the input buffer into complex-valued wave fields as wave-modeled prompting data;

contemporaneously pre-processing the prompting data and assigning phase values;

using wave propagation to transport the wave-modeled prompting data to the cortex to prompt a response from the cortex;

mathematically operating upon the previously stored associations at the cortex using a de-association function that is the inverse of that originally used to form the associations;

propagating the result of the mathematical de-association operation, representing a retrieval, to one or more IIP buffers;

autonomously reading a retrieved pattern as accurately as possible;

deducing an identification code that could correspond to a previously created IIP;

generating a confidence estimate based on a relative certainty or uncertainty of the identification made;

recalling the associated files or other information related to the reported identification code and displaying the results in human or machine-readable form;

executing or communicating the appropriate commands based on the identification code, the reported confidence estimate, and the predefined confidence levels required for the relevant commands;

adaptively improving identification performance in response to feedback on the accuracy of past identifications, using the following equation for the case of false positive identifications:

$$C_{new} = C_{old} - \beta_i \langle R_i, I_j \rangle$$

where C_{old} is the original cortex value, C_{new} is the revised cortex value, β_i is a positive weighting factor, R_i is the prompting pattern, and I_j is the incorrectly retrieved IIP and using the following equation for the case of false negative or overly weak positive identifications:

$$C_{new} = C_{old} + \beta_i \langle R_i - \gamma_i P_i, I_i \rangle$$

where C_{old} is the original cortex value, C_{new} is the revised cortex value, β_i is a positive weighting factor, R_i is the prompting pattern, I_i is the desired IIP, P_i is the original pattern associated with I_i, and γ_i is 0 for augmentation mode and 1 for replacement mode.

75. The method of autonomous pattern recognition of Claim 74, wherein the method of information transport is by propagating physical waves using antenna arrays and supporting hardware and software.

76. The method of autonomous pattern recognition of Claim 75, wherein the method of information transport is by simulating wave propagation in computer hardware configured by computer software or wave propagation circuitry in which sets of data are input, pre-processed, and then represented as wave functions $\xi_i(\mathbf{r})$ that are time-harmonic solutions to the wave equation:

$$\left(\nabla^2 + k^2\right)\xi_i(\mathbf{r}) = 0;$$

in which the propagation of a wave away from a surface such as a buffer or the cortex is formally and exactly described by the Kirchhoff integral:

$$\xi_i(\mathbf{r}) = \oiint_{S_C} d\mathbf{S}_C \cdot \{\xi_i(\mathbf{r}_C)\nabla_C G(\mathbf{r},\mathbf{r}_C) - G(\mathbf{r},\mathbf{r}_C)\nabla_C \xi_i(\mathbf{r}_C)\}$$

where the surface S_C is closed and completely surrounds a destination point $\mathbf{r}$, the gradient operates only on coordinates on the source surface S_C, and $G(\mathbf{r},\mathbf{r}_C)$ is a Green's function; and in which the above continuous integral is discretized for numerical implementation as:

$$\xi(\mathbf{r}) = \sum_{\text{all source points}} \Delta\mathbf{S}_C \cdot \{\xi(\mathbf{r}_C)\nabla_C G(\mathbf{r},\mathbf{r}_C) - G(\mathbf{r},\mathbf{r}_C)\nabla_C \xi(\mathbf{r}_C)\}$$

thus enabling digital input, output, and computation.

77. The method of autonomous pattern recognition of Claim 75, wherein the patterns recognized represent physical or electronic stimuli.

78. The method of autonomous pattern recognition of Claim 77, wherein the physical or electronic stimuli represent images, human faces, sounds, fingerprints, signatures, gas molecules, or chemical compositions.

IX. EVIDENCE APPENDIX (37 C.F.R. 41.37(c)(9))

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X. RELATED PROCEEDINGS APPENDIX (37 C.F.R. 41.37(c)(10))

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If any applicable fee or refund has been overlooked, the Commissioner is hereby authorized to charge any fee or credit any refund to the deposit account of Jackson Walker L.L.P., No. 10-0096.

Respectfully submitted,

By: _____
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